Amendments to the Claims:

Please cancel claims 2, 25, 34, 37, 44, and 48 and amend claims 1, 3-5, 8-10, 12-18, 20-24, 26-33, 35, 36, 38-43, 45-47, 49-53, and 55 as follows:

1. (Currently Amended) A method for improving digital testing of an analogue or mixed-signal circuit, the method comprising:

inputting a digitized input test sequence to a fault free version of the analogue or mixed signal circuit or computer simulation thereof;

inputting the same digitized input test sequence to a version of the circuit or computer simulation thereof that has at least one specified fault,

using an optimization algorithm to vary the input test sequence;

monitoring the outputs of the fault free and faulty circuits for each test sequence; and

identifying an optimized digitized input test sequence, wherein the optimized digitized input test sequence is used to identify a corresponding digitized output for use in a test mode

~~optimising an input digital test signal~~.

2. (cancelled).

3. (Currently Amended) A method as claimed in claim 1 ~~claim 2~~ comprising for each input, determining a measure~~, for example a figure of merit,~~ that is indicative of differences between the output of the fault free circuit and the output of the known faulty circuit in response to the digitized input test sequence ~~digital input signal~~ and selecting an improved input digitized test sequence ~~signal~~ based on the determined measures for all of the sequences ~~input digital signal~~.

4. (Currently Amended) A method as claimed in claim 1 ~~claim 2~~, wherein varying the initial digitized input test sequence is done ~~the step of applying a plurality of digital input signals involves applying an initial signal and then varying that~~ according to pre-determined

criteria.

5. (Currently Amended) A method as claimed claim 4, wherein the step of varying the initial digitized input test sequence ~~digital signal~~ involves changing the length of one or more individual pulses in the sequence ~~that signal~~.

6. (Original) A method as claimed in claim 5, wherein the length of individual pulses is varied by the same amount or by increasingly large or small amounts or by different amounts, which different amounts may be selected randomly or according to predefined criteria.

7. (Original) A method as claimed in claim 6, wherein the length of all of the pulses is varied by the same amount in sequence one after the other.

8. (Currently Amended) A method as claimed in claim 6 ~~claim 7~~ further involving changing the size of the amount by which the pulse lengths are varied and repeating the process of varying.

9. (Currently Amended) A method as claimed in claim 4, wherein varying the digitized input test sequence ~~the process of varying the input digital signal~~ involves inputting ~~applying~~ a pre-determined function to the initial input sequence, ~~such as a pattern shift function~~, which function ~~in effect~~ modifies simultaneously all pulses in the digitized input test sequence ~~pattern~~ at once.

10. (Currently Amended) A method as claimed in claim 1 ~~claim 2~~ comprising inputting ~~applying~~ a range of different initial digitized input test sequences ~~digital inputs~~, each of these being varied according to pre-determined criteria to find a local optimum for each initial input.

11. (Original) A method as claimed in claim 10 comprising comparing all of the local optima and selecting the optimum signal.

12. (Currently Amended) A method as claimed in claim 1 ~~claim 2~~, wherein the monitored outputs ~~signals used~~ for each of the fault free circuit and the known faulty circuit are analogue outputs.

13. (Currently Amended) A method as claimed in claim 12 comprising processing the~~, wherein the~~ analogue outputs ~~signals are processed~~ to prevent domination of large differences in the output prior to selection of the digitized input test sequence ~~optimum input signal~~.

14. (Currently Amended) A method as claimed in claim 13, wherein processing ~~of~~ the analogue signals involves using a function having an output that saturates at two different predetermined values for extreme negative and positive values of input.

15. (Currently Amended) A method as claimed in claim 14, wherein the function is a sigmoidal function, which employs a non-linear squashing function based on the sigmoid or logistic equation, wherein ~~preferably~~ the sigmoidal function is a hyperbolic tan function.

16. (Currently Amended) A method as claimed in claim 1, wherein digitized ~~digital~~ outputs from the fault free and the faulty circuits are used to determine the optimum digitized ~~digital~~ input test signal.

17. (Currently Amended) A method as claimed in claim 1 further comprising using ~~, wherein~~ a fault detection ratio ~~is used~~ to determine the digitized input test sequence, ~~optimum circuit, this~~ the fault detection ratio being defined as the proportion of a set of predefined faults that can be detected according to a set of criteria for fault discrimination.

18. (Currently Amended) A method as claimed in claim 17 ~~claim 3~~, wherein the fault detection ratio ~~figure of merit~~ is the Hamming distance between the digitized ~~digital~~ output response for the fault free circuit and the digitized output response for the faulty circuit.

19. (Original) A method as claimed in claim 18, wherein the figure of merit is proportional to or a function of the Hamming distance.

20. (Currently Amended) A method as claimed in claim 1 comprising using ~~, wherein an exhaustive evaluation of~~ a pre-determined group of possible digitized input test ~~digital~~ sequences ~~is used~~ to find one or more good initial or starting digitized ~~digital~~ input sequences.

21. (Currently Amended) A method as claimed in claim 1 ~~claim 2~~, wherein rather than optimizing ~~optimising~~ the digitized input test sequence ~~signal~~ based on known faults, the signal is optimized ~~optimised~~ to take into account variations in values of functional specifications.

22. (Currently Amended) A method as claimed in claim 1, wherein the using an optimization algorithm uses an optimization algorithm that is selected from at least one of a hill climbing algorithm and a genetic algorithm. ~~step of optimising the digital test input is implemented using an optimisation algorithm, for example a hill-climbing algorithm and/or a genetic algorithm or modified version of one of these~~

23. (Currently Amended) A digitized input test sequence ~~digital test signal~~ or a copy thereof for testing analogue or mixed signal circuits that is a product of: ~~the method of claim 1~~

inputting a digitized input test sequence to a fault free version of the analogue or mixed signal circuit or computer simulation thereof;

inputting the same digitized input test sequence to a version of the circuit or computer simulation thereof that has at least one specified fault,

using an optimization algorithm to vary the input test sequence;

monitoring the outputs of the fault free and faulty circuits for each test sequence; and

identifying an optimized digitized input test sequence, wherein the optimized digitized input test sequence is used to identify a corresponding digitized output for use in a test mode.

24. (Currently Amended) A system for improving digital testing of an analogue or mixed-signal circuit, the system being configured to:

input a digitized input test sequence to a fault free version of the analogue or mixed signal circuit or computer simulation thereof;

input the same digitized input test sequence to a version of the circuit that has at least one specified fault;

use an optimization algorithm to vary the input test sequence;

monitor the outputs of the fault free and faulty circuits for each test sequence and identify a digitized input sequence, wherein the digitized input is used to identify a corresponding digitized output for use in a test mode ~~comprising means for optimising an input digital test signal, preferably wherein the means for optimising comprise an optimisation algorithm, such as a hill-climbing algorithm and/or a genetic algorithm or a modified version of one of these~~.

25. (Cancelled)

26. (Currently Amended) A system as claimed in claim 24 ~~claim 25~~ operable to determine a measure that is ~~comprising means for determining a measure, for example a figure of merit, that is~~ indicative of differences between an output of the ~~a~~ fault free circuit and an output of the known faulty circuit in response to a digitized input test sequence, and select the ~~digital input signal, wherein the means for selecting the~~ optimum digitized input test sequence ~~signal is operable to do so~~ based on the measures determined for each digitized input test sequence ~~digital signal~~.

27. (Currently Amended) A system as claimed in claim 24~~, wherein the means for applying a plurality of digital input signals are~~ operable to input an initial digitized input test

sequence ~~apply an initial signal~~ and then vary the digitized input test sequence ~~that~~ according to pre-determined criteria.

28. (Currently Amended) A system as claimed in claim 27~~, wherein the means for applying are~~ operable to vary the initial digitized input test sequence ~~digital signal~~ by changing the length of one or more individual pulses in ~~that~~ the digitized input test sequence ~~signal~~.

29. (Currently Amended) A system as claimed in claim 28~~, wherein the means for applying are~~ operable to vary the pulse length by one of the same amount ~~or by~~; an increasingly large amount; an increasingly small amount, and ~~or small amounts or by~~ different amounts, which different amounts are either ~~may be~~ selected randomly or by predefined scheme.

30. (Currently Amended) A system as claimed in claim 24, wherein the system is operable ~~means for applying are operable~~ to vary the frequency of the digitized input test sequence using the optimization algorithm ~~digital signal~~.

31. (Currently Amended) A system as claimed in claim 24, wherein the system is ~~means monitoring are~~ operable to monitor analogue outputs from the fault free and faulty circuits.

32. (Currently Amended) A system as claimed in claim 24, wherein the system is ~~means monitoring are~~ operable to monitor digitized ~~digital~~ outputs from the fault free and faulty circuits.

33. (Currently Amended) A system as claimed in claim 24, wherein the system is operable to determine ~~further comprising means for determining~~ a figure of merit for each one of a plurality of different faulty circuits and determining a composite figure of merit combining all of these.

34. (Cancelled)

35. (Currently Amended) A method for testing analogue and/or mixed-signal circuits using a digitized sequence, ~~digital signal,~~ the method comprising:

inputting ~~applying~~ to the circuit under test an ~~optimised~~ optimized digitized test sequence ~~signal~~ as claimed in claim 23;

comparing ~~an~~ a digitized output of the circuit under test with an expected digitized output for a fault free circuit; and

determining a fault based on a result of the step of comparing.

36. (Currently Amended) A method as claimed in claim 35, wherein the output from the circuit under test and the expected output are analogue, and the method further involves digitizing the output of the circuit under test wherein the expected output for the fault free circuit includes an acceptable tolerance range for the optimized input test sequence.

37. (Cancelled)

38. (Currently Amended) A method as claimed in claim 35, wherein the expected output for the fault free circuit includes an acceptable tolerance range for the ~~optimised~~ optimized digitized input test sequence ~~signal~~.

39. (Currently Amended) A method as claimed in claim 35 further comprising storing outputs for one or more known faults for the optimized digitized ~~optimised digital~~ test sequence ~~signal~~ and comparing an output from a circuit under test with these.

40. (Currently Amended) A method as claimed in claim 39, wherein the stored outputs for the one or more known faults include an acceptable tolerance range for the optimized digitized ~~optimised~~ input test sequence ~~signal~~.

41. (Currently Amended) A method as claimed in claim 35 wherein in the event that a ~~the~~ gain of the circuit is to be tested, the digitized input ~~digital~~ test sequence ~~signal~~ has an optimized ~~optimised~~ offset voltage and/or amplitude.

42. (Currently Amended) A system for testing analogue and/or mixed-signal circuits using a ~~digital signal~~ digitized input test sequence, the system comprising:

means for inputting ~~applying~~ to the circuit under test an optimized digitized input sequence ~~optimised test signal~~ as defined in claim 23;

means for comparing an output signal of the CUT with an expected output signal for a good circuit; and

means for determining a fault based on an output from the means for comparing.

43. (Currently Amended) A system as claimed in claim 42, wherein the outputs from the CUT are analogue, and means are provided for digitizing the outputs of the circuit under test.

44. (Cancelled)

45. (Currently Amended) A system as claimed in claim 42, wherein the means for inputting comprises a single ~~digital signal~~ sequence generator is provided for stimulating a plurality of different electronic functions or sub-systems.

46. (Currently Amended) A system as claimed in claim 42 ~~claim 45~~, wherein the means for determining a fault comprises a single detector that is operable to analyze outputs ~~analyse output~~ ~~signals~~ from each of the plurality of different electronic functions or sub-systems.

47. (Currently Amended) A computer program for improving testing of an analogue or mixed-signal circuit using a digitized input test sequence ~~digital signal~~, the computer program being provided ~~preferably~~ on a data carrier or computer readable medium and having code or instructions for: ~~optimising an input digital test signal~~

inputting a digitized input test sequence to a fault free version of the analogue or mixed signal circuit or computer simulation thereof;

inputting the same digitized input test sequence to a version of the circuit that has at least one specified fault;

using an optimization algorithm to vary the input test sequence;

monitoring the outputs of the fault free and faulty circuits for each digitized input test sequence; and

identifying a digitized input sequence, wherein the digitized input is used to identify a corresponding digitized output for use in a test mode.

48. (Cancelled)

49. (Currently Amended) A computer program as claimed in claim 47 ~~claim 48~~ comprising code or instructions for determining, for each ~~digital~~ digitized input test sequence ~~signal~~, a measure~~, for example a figure of merit,~~ that is indicative of differences between an output of a fault free circuit and an output of known faulty circuit in response to a ~~digital~~ digitized input test sequence ~~signal~~ and selecting an optimum digitized input test sequence ~~signal~~ based on the determined measures for each digitized input test sequence ~~digital signal~~.

50. (Currently Amended) A computer program ~~may~~ as claimed in claim 47 having code or instructions for modelling output responses for the fault free version of the analogue or mixed signal circuit and the version of the circuit that has at least one specified fault ~~faulty circuits~~.

51. (Currently Amended) A computer program for use in a method of testing an analogue or mixed-signal circuit using a ~~digital signal~~ digitized input test sequence, the computer program being provided ~~preferably~~ on a data carrier or computer readable medium and having code or instructions for:

inputting ~~applying~~ to a circuit under test an optimized digitized test sequence ~~a test signal~~

as ~~determined using the method~~ defined in claim 23 ~~claim 1~~;

comparing an output signal of the circuit under test with an expected output signal for a good circuit; and

determining whether there is a fault based on an output from the instructions ~~means~~ for comparing.

52. (Currently Amended) A computer program as claimed in claim 51 having code or instructions for storing a measure~~, for example a figure of merit,~~ for a circuit having a known fault and comparing the measure for the circuit under test with that for the known fault.

53. (Currently Amended) A test system that includes means for generating an ~~optimised digital~~ optimized digitized test ~~signal~~ input sequence as ~~determined using the method~~ defined in claim 23 ~~claim 1~~, means for inputting ~~applying~~ the ~~digital~~ digitized input test sequence ~~signal~~ to an analogue or mixed-signal circuit under test, means for comparing an output signal of the circuit under test with an expected output signal for a known circuit~~, for example a fault free circuit or a known faulty circuit,~~ which is also stored or generated locally, and means for determining a fault based on an output from the means for comparing.

54. (Original) A test system as claimed in claim 53 that is provided on the same chip as the circuit under test.

55. (Currently Amended) An electronic device~~, such as a mobile telephone,~~ that includes a test system that has means for generating an ~~optimised digital~~ optimized digitized input test signal ~~as determined using the method~~ as defined in claim 23 ~~claimed in claim 1,~~ means for ~~applying~~ inputting the ~~digital~~ digitized input test sequence ~~signal~~ to an analogue or mixed-signal circuit under test, means for comparing an output signal of the circuit under test with an expected output signal for a good circuit, which is also stored or generated locally, and means for determining a fault based on an output from the means for comparing.